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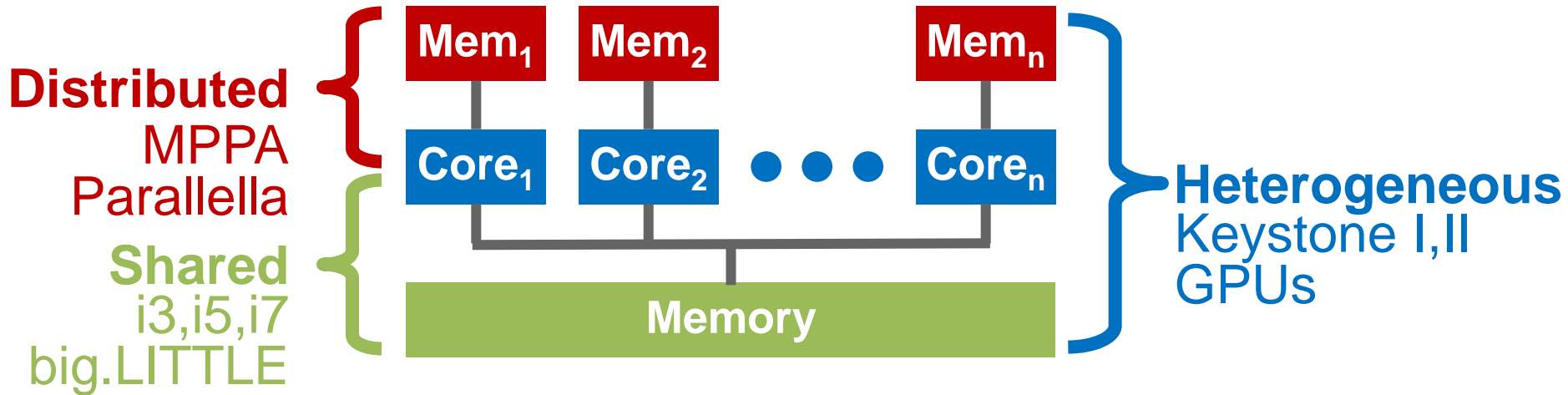
DISTRIBUTED MEMORY ALLOCATION TECHNIQUE FOR SYNCHRONOUS DATAFLOW GRAPHS

**Karol DESNOS, Maxime PELCAT,
Jean-François NEZAN, Slaheddine ARIDHI**

SiPS – Dallas (TX), USA – Oct. 26th 2016



Architects: *Distributed is the new shared!*



Embedded Software Engineer: *Distribu-what?*

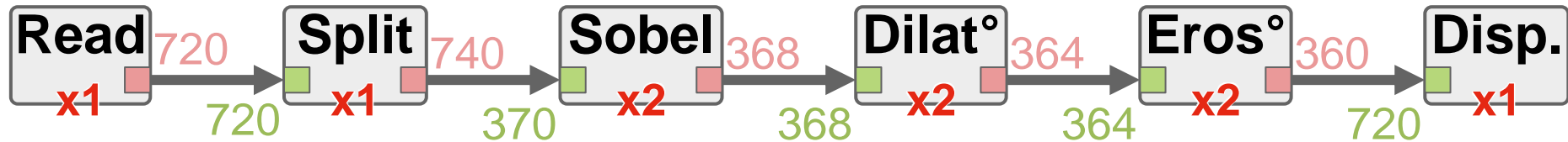
- **Shared memory parallel APIs:**
(P)threads, OpenMP, Cilk, Threading Building Blocks, ...
- **Distributed memory APIs**
MPI, Go lang → **Mostly for HPC**

New distributed memory allocation technique:

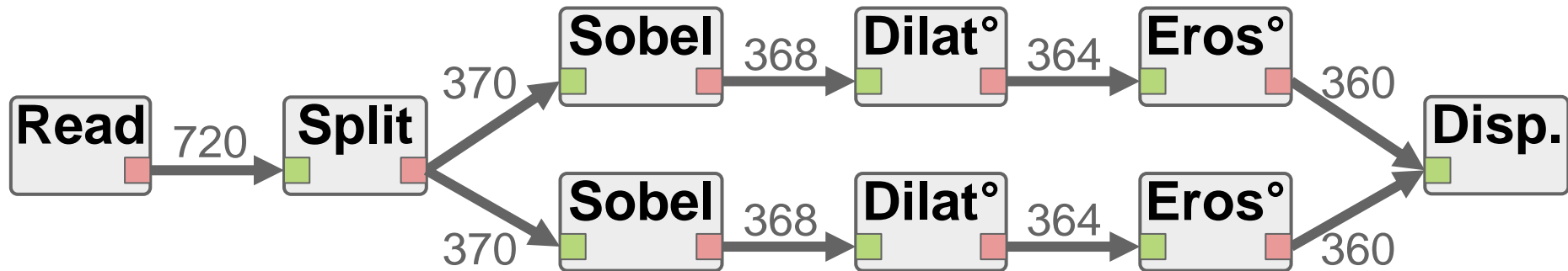
- **Parallel:** Application described with SDF graphs.
- **Simple:** Fully automated.
- **Flexible:** Shared / heterogeneous / distributed architectures.
- **Efficient:** Memory footprint minimization with memory reuse.
- **Performant:** Improve application performance.

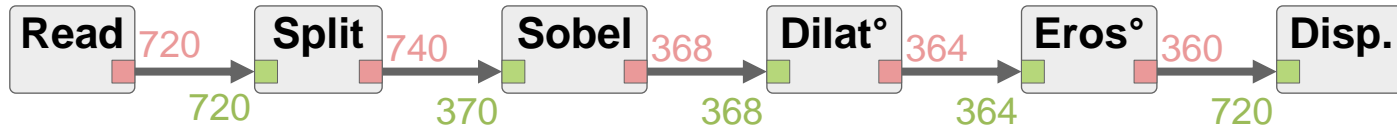
Synchronous Dataflow (SDF) Graph

- Actors and data ports
 - FIFO Queues
- ➔ Data driven execution**

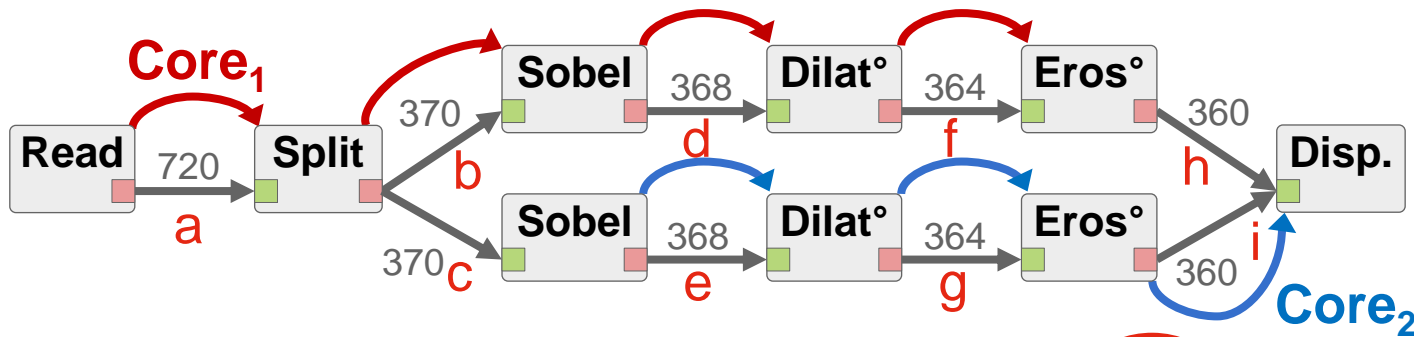


Equivalent single-rate SDF graph



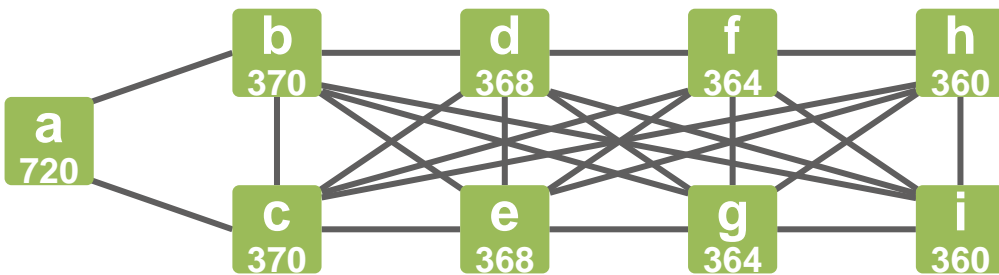


1 Transform



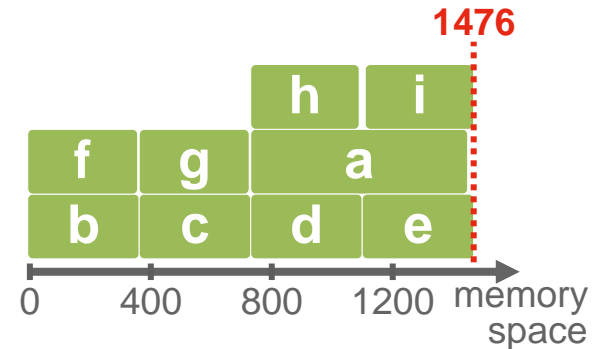
2 Model

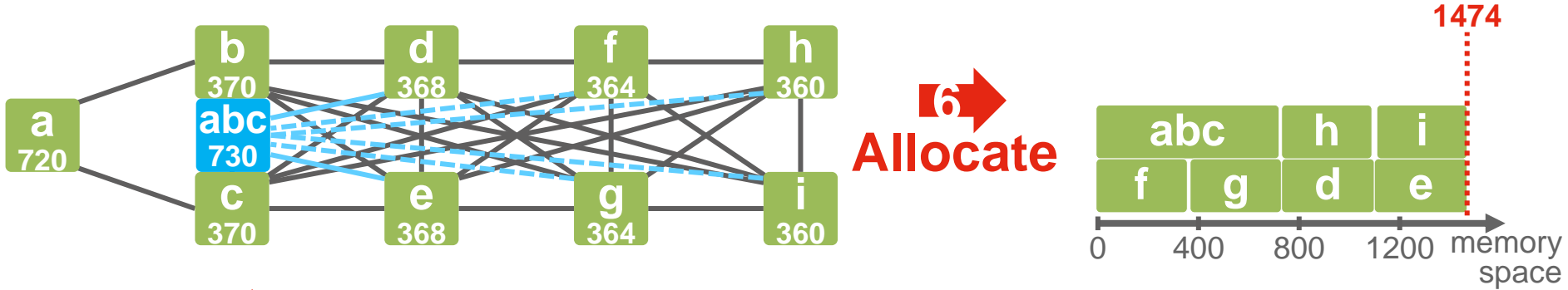
3 Update



Memory Exclusion Graph (MEG)

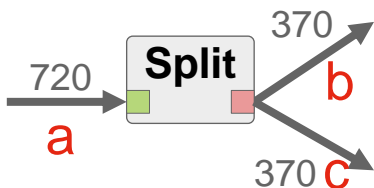
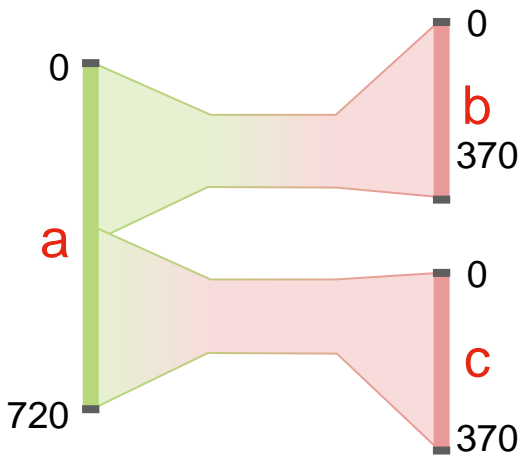
6 Allocate

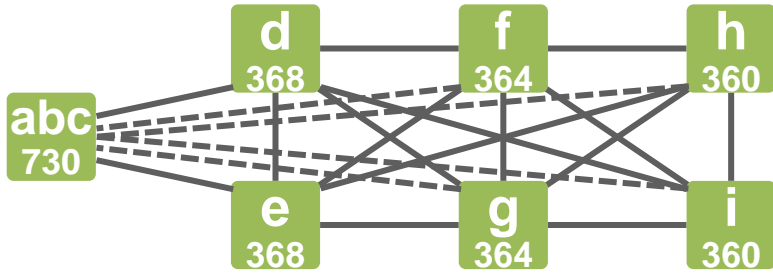




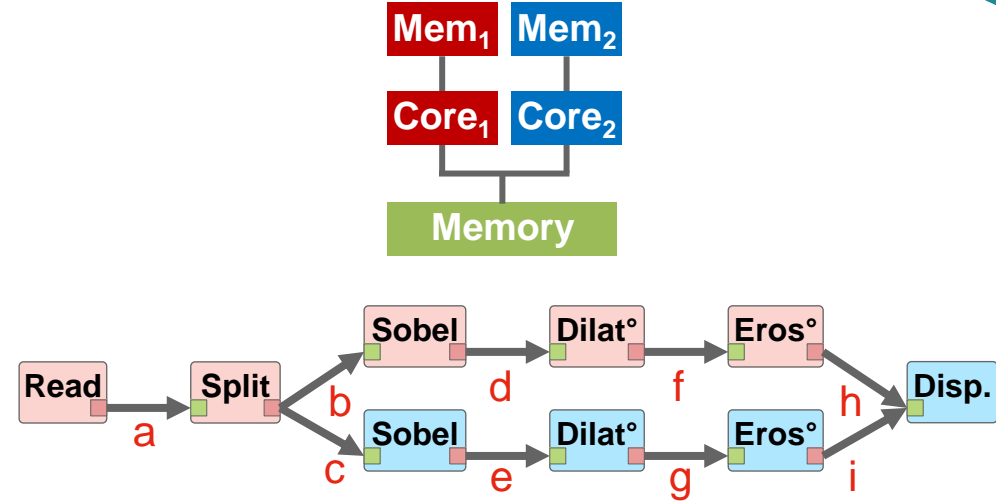
6 Allocate

4 Merge

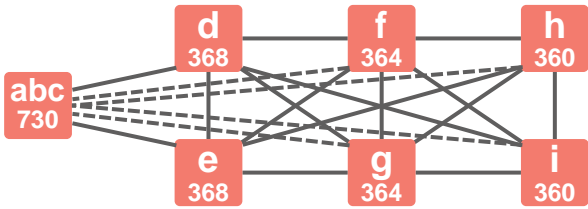




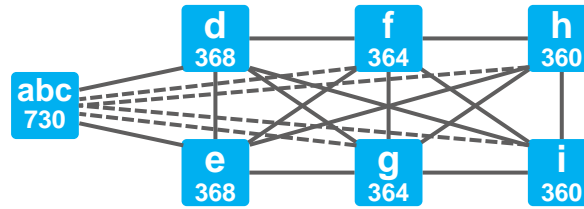
5 Distribute



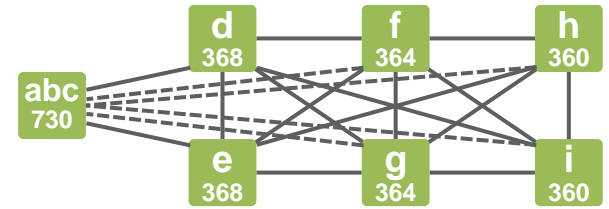
Mem₁



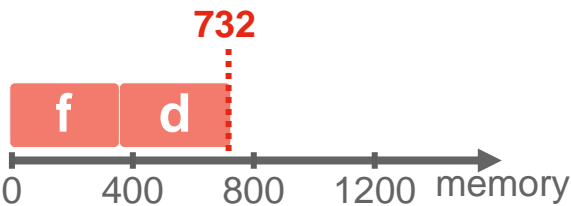
Mem₂



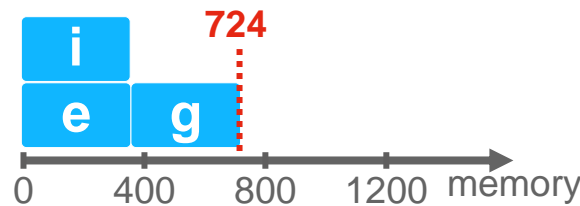
Shared



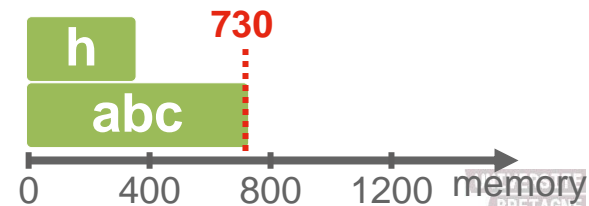
6

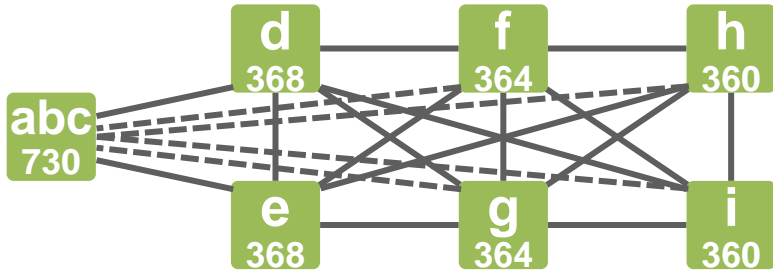


6 Allocate

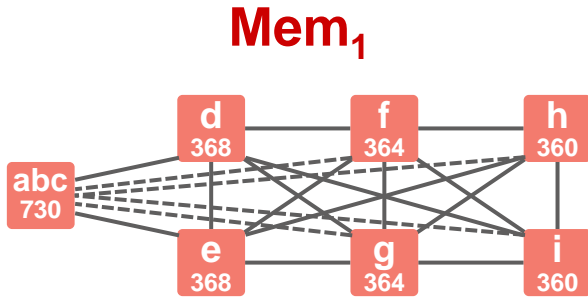


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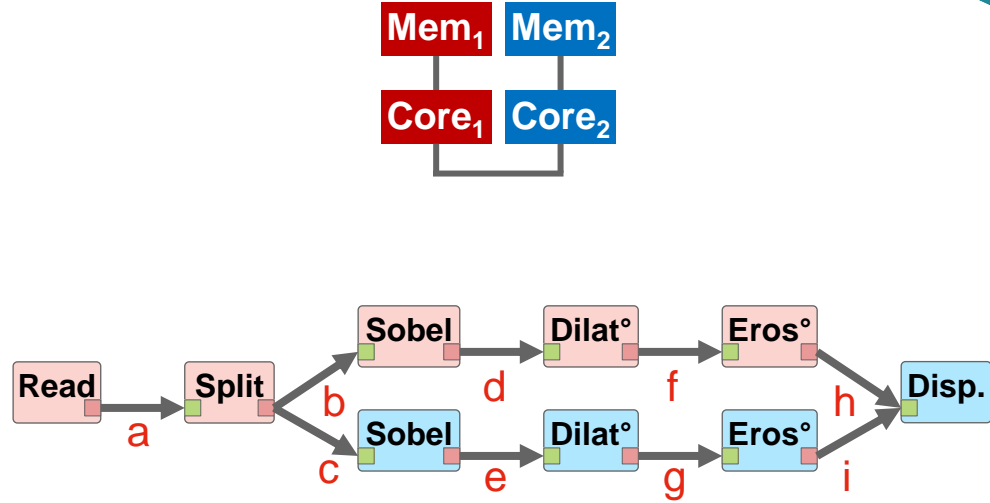
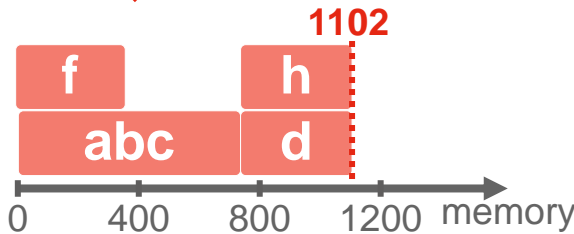




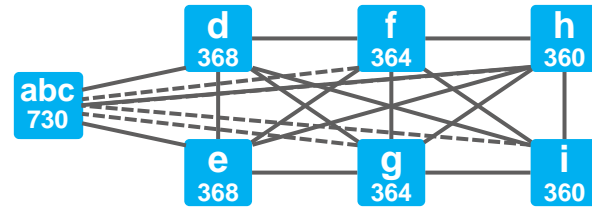
5 Distribute



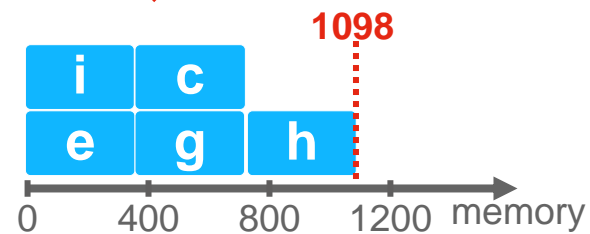
6 Allocate

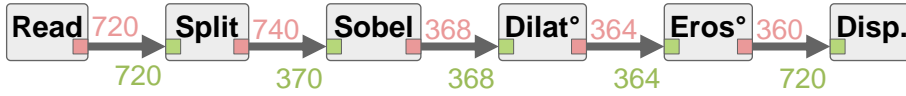


Mem₂

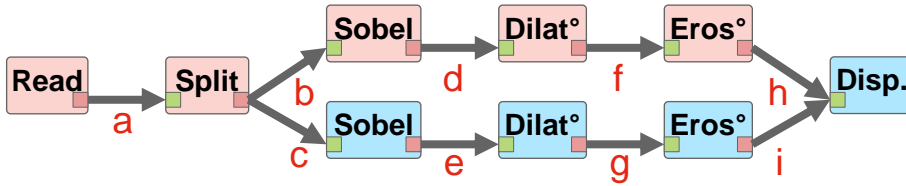


6



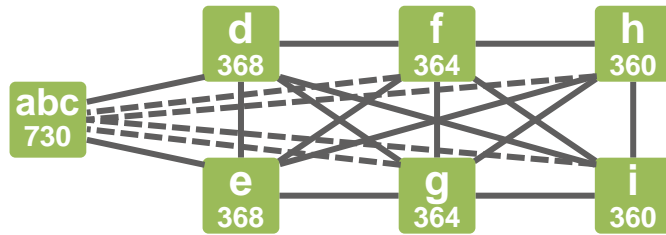


1 Transform

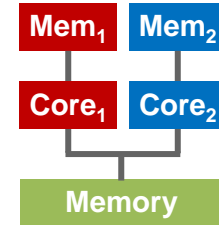
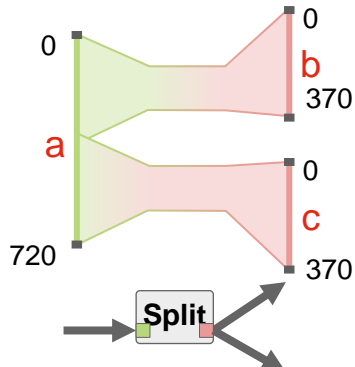


2 Model

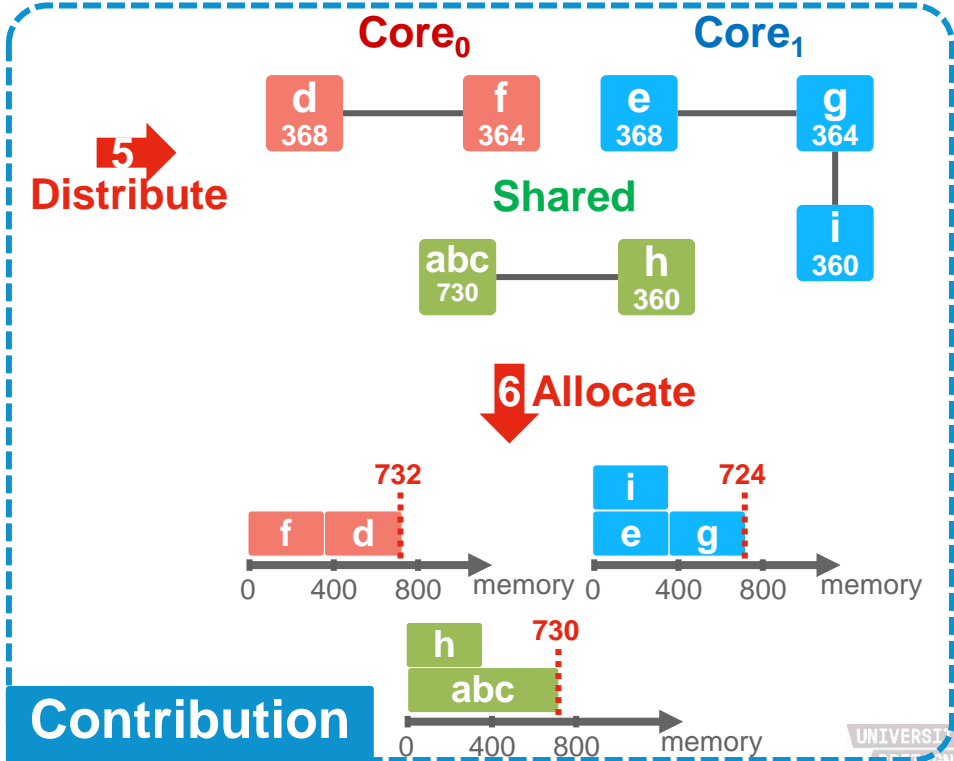
3 Update



4 Merge



5 Distribute



6 Allocate

Contribution

- **PREESM**

- Rapid prototyping framework
- Open-source → Reproducibility



- **Texas Instruments C6678**

- 8 DSP cores
- Heterogeneous memories:
 - Optional L1 caches: 32 kBytes / core
 - Distributed memories: 512 kBytes / core
 - Shared memory: 512 Mbytes



- **Computer vision algorithms**

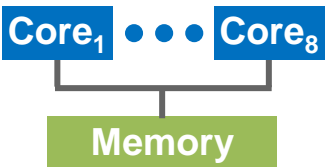
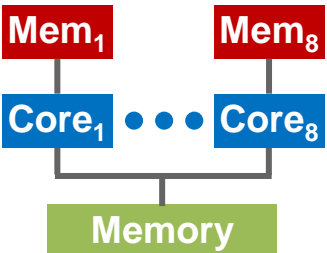


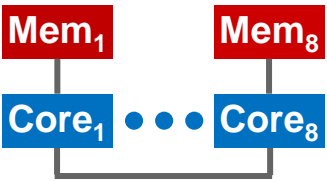

- Sobel & morphological operations
- Stereo Matching:
 - 28 actors, 42 FIFOs, 1067 buffers



Left ↓ Right



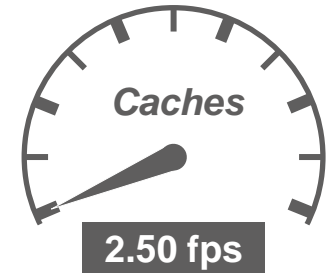
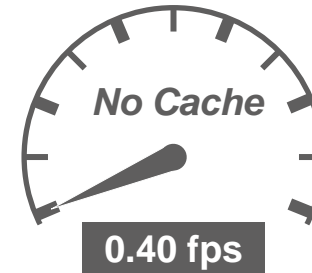
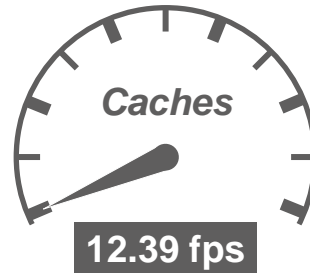
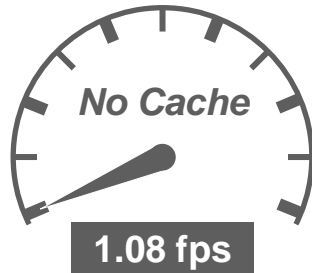
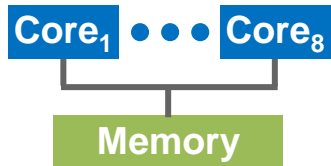
Depth map

| | Sobel | Stereo | | | | | | | | |
|--|--|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| <p>Shared</p>  | <p>3800kB</p> | <p>5.50 MB</p> | | | | | | | | |
| <p>Heterogen.</p>  | <p style="color: red;">240kB</p>  <p>total: 4320kB</p> | <p style="color: red;">0.21 MB</p> <p style="color: red;">0.31 MB</p>  <p>total: 6.81 MB</p> | | | | | | | | |
| <p>Distributed</p>  | <p style="color: red;">248kB</p>  <p>total: 5688kB</p> | <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="background-color: red; color: white; text-align: center;">4.32 MB</td> <td style="background-color: red; color: white; text-align: center;">4.09 MB</td> </tr> <tr> <td style="background-color: red; color: white; text-align: center;">4.30 MB</td> <td style="background-color: red; color: white; text-align: center;">4.20 MB</td> </tr> <tr> <td style="background-color: red; color: white; text-align: center;">4.43 MB</td> <td style="background-color: red; color: white; text-align: center;">4.40 MB</td> </tr> <tr> <td style="background-color: red; color: white; text-align: center;">3.78 MB</td> <td style="background-color: red; color: white; text-align: center;">4.07 MB</td> </tr> </table> | 4.32 MB | 4.09 MB | 4.30 MB | 4.20 MB | 4.43 MB | 4.40 MB | 3.78 MB | 4.07 MB |
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| 4.43 MB | 4.40 MB | | | | | | | | | |
| 3.78 MB | 4.07 MB | | | | | | | | | |

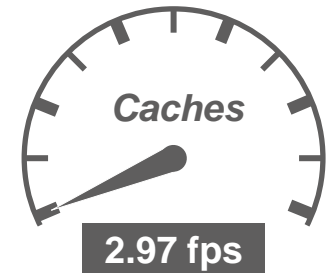
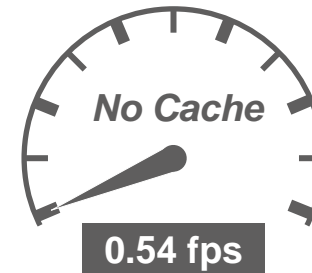
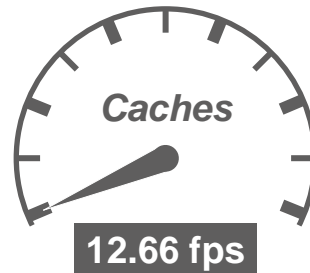
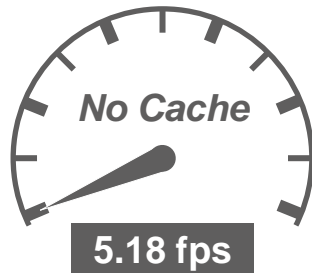
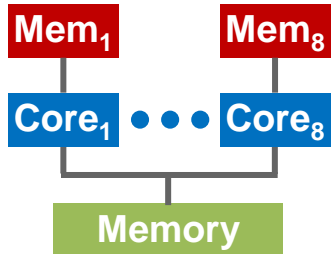
Sobel

Stereo

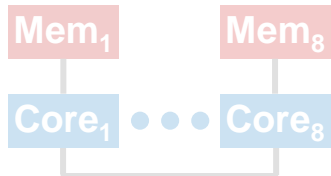
Shared



Heterogen.



Distributed



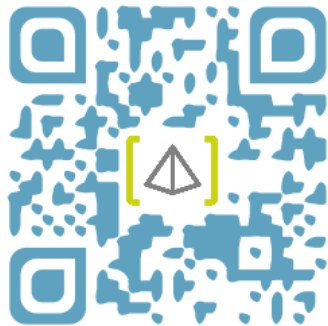
Distributed code generation: Future work

New distributed memory allocation technique:

- **Parallel:** SDF Graph
- **Simple:** Automated
- **Efficient:** Memory reuse
- **Performant:** Applications
- **Flexible:** Memory architectures

Future work

- Code generation for distributed architecture (W.I.P)
- Memory aware mapping/scheduling



<http://preesm.sf.net>



@PreesmProject